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(54) Phase locked loop arrangement.

(57) The invention can be used to extract information in a Synchronous Digital Hierarchy (SDH) transmission system and relates to the extraction of information from a PCM data stream. It is desirable to provide a Dual Filtering Method for a System having dual data rate justification in a simple manner using minimum components. To obtain a relatively simple circuitry a single controlled oscillator source is used to time the data output stream.

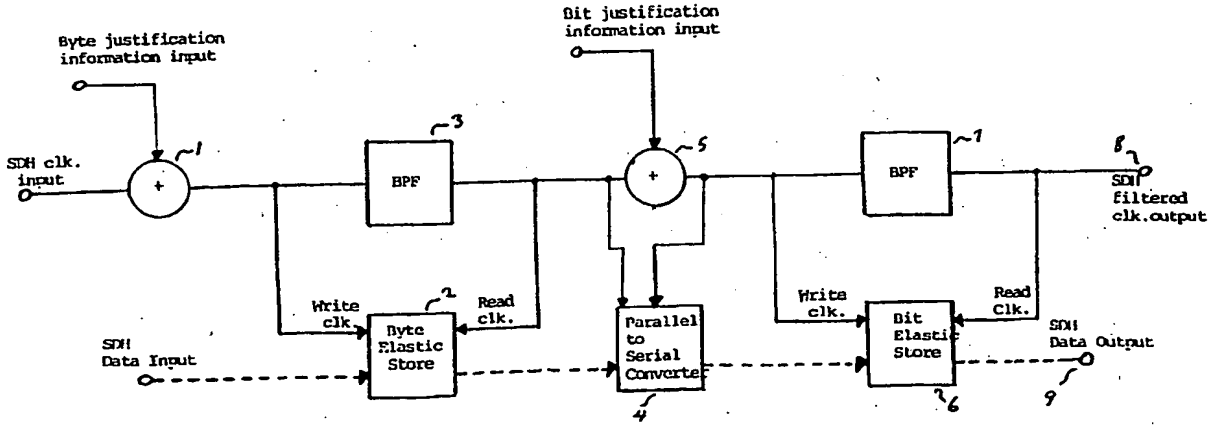

Fig 1.

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This invention relates to the extraction of information from a PCM data stream. In a particular r application the invention can be used to extract information in a Synchronous Digital Hierarchy (SDH) transmission system.

The extraction of information from such a system can be equated to the recovery of clock signals from a data stream composed of signals from a plurality of clock sources.

In an SDH system the data stream may include eg. frame clocks, byte clocks, and bit clocks each conveying different manifestations of information.

Within the known SDH range of equipment described in CCITT recommendations G707, 708 and 709 there is provision for possible clock frequency differences caused by the plesiochronous nature of the digital telephone network. These differences are processed using a so-called floating mode of operation within the hierarchy, as described in the aforementioned CCITT recommendation G709. With the floating mode of operation two methods of data rate justification are used for clock correction, viz. Byte mode justification for those clock differences apparent within a network of SDH equipment; and bit mode justification for those clock differences apparent at tributary interface points where external networks connect to the SDH equipment network. The resultant sum of these justification processes must be processed at the tributary output ports and this is usually done using one or more elastic stores (FIFO) together with phase locked read clocks to prevent loss of data while attenuating framing and justification jitter present at the tributary output ports. The store can be implemented also by other suitable known stores such as a RAM. In one embodiment the invention may be used to handle packet data where different packets may arrive out of order due to different transmission paths. In such a case the store could be implemented by the use of a RAM from which the packet data could be read out in the correct sequence.

Designs presently exist for phase locked loops which provide filtering means similar to that required by SDH equipment (see British Telecom's submission T1X1 6/89 entitled "SONET Desynchronisers") but these designs are either excessively complex or lack flexibility in processing the dual justification referred to above.

Each of the two aforementioned justification methods have different requirements; the first justification method, being byte mode in nature, but restricted within the SDH network where clock frequency differences will be small, will have characteristics of low frequency large amplitude (8 bit) phase hits which require considerable smoothing to maintain performance required by equipment having interfaces designed in accordance with CCITT G703 recommendations and jitter tolerance specifications in accordance with limits set in the CCITT G823 recommendations. The second justification method, being bit mode in nature, and having characteristics of the network external to the SDH network, requires a fast response time enabling quick settling times from transient error and changeover related conditions occurring outside the SDH equipment.

The aforementioned British Telecom submission proposes dual elastic stores and phase locked oscillators to provide these dual justification processing methods, but the complexity of the circuitry required to implement the arrangement proposed in the British Telecom submission is obvious.

It will be understood that compromise arrangements can be designed which have simpler circuitry but performance will be sacrificed. For example a single phase locked loop could be utilised but it would require filter characteristics to meet the most severe jitter source equivalent to the Byte Mode justification referred to above. Speed of response and settling time imposed on the smoothing of the bit mode justification would be sacrificed.

It is desirable to provide a dual filtering method for a system incorporating dual data rate justification in a relatively simple manner. Broadly, the inventive method comprises

storing two or more bytes of the input data as it is received in buffer store means,

calculating the time average over a first period of time at which the input data is received,

and generating an output clock to feed the data out of the store at an output pulse rate which over a second period of time has the same time average as the input data bit rate,

wherein the input data rate is subject to two or more sources of fluctuation, and wherein the output pulse rate can be selectively adjusted in response to the source of the fluctuation.

In particular the method can be used to extract data at a rate approximating the input rate after the input data has been multiplexed with other data and transmitted at a higher data rate.

This specification describes a method of providing a controlled response from each of a plurality of clock sources to a single controlled oscillator means using independently sensed information signals from each clock source, each clock source contributing to a total data process forming a data stream whose rate requires filtering by the controlled oscillator means, said method comprising the steps of:

1. Monitoring each said clock source for transient conditions.

2. Generating a response characteristic for each monitored clock source.

3. Summing the results of the characteristics so generated to obtain a total modifying function.
4. Obtaining a total phase difference signal between the data stream to be filtered and the controlled oscillator means' output.
5. Adding the total modifying function to the total phase difference to produce a modified phase function.
6. Processing the modified phase function to produce a control signal for application to said controlled oscillator means.

Preferably the plurality of clock sources comprise a basic clock means containing framing gaps, and other clocks generated by bit and/or byte justification information data.

Preferably, the data stream is recovered by combining the basic clock means and the justification clocks in accordance with relevant information bits exiting from a preceding transmission source. The justification clocks indicate when optional bits or bytes should be omitted or included, depending on whether the bit or byte contains data or justification.

Preferably, the total phase difference signal is obtained by subtracting the read address from the write address of an elastic store means used to buffer the data stream as it is processed by the sum of the basic clock means and the justification clocks forming the write clock, and the controlled oscillator means output forming the read clock. This is an indication of the different rates at which data is written into and read from the store. The read clock can be adjusted accordingly.

A phase locked loop oscillator may be implemented from the method of the invention which exhibits bandpass filtering characteristics differing on the basis of at least two independent controlling sources. The characteristics may be cascaded or paralleled to produce a variety of filtering combinations.

The specification also discloses an arrangement for adjusting the local data rate to accommodate the data rate of an incoming data stream which includes byte justification information and bit justification information, the arrangement comprising:

first adder means for adding the byte justification information to the incoming data byte clock information,

the output of the first adder means being applied to byte elastic store means as the byte input clock,

the data from the incoming data stream being fed into the elastic store means under the control of the byte input clock,

the byte elastic store including a store fill status output indicating the level of the contents of the elastic store,

the byte justification information being applied to a first coefficient generator which produces an output corresponding to the rate of byte justification insertion in relation to the data byte rate,

combining means to combine the output of the first coefficient generator and the store full status output,

the output of the combining means being applied to a second coefficient generator which controls the frequency of a local clock oscillator to bring the frequency of the local clock oscillator closer to synchronism with the bit clock rate of the incoming data,

the output of the local clock oscillator is combined with the bit justification and controls the reading of data from the elastic store into a byte/bit converter,

the data being read from the byte/bit converter under the control of the output of the local clock oscillator.

Also disclosed is a method for adjusting the local clock data rate to accommodate the data rate of an incoming data stream which includes byte justification information and bit justification information, the method comprising:

adding the byte justification information to the incoming data byte clock information to produce a first control clock signal,

storing the incoming data in an elastic store under the control of the first control clock signal,

deriving a store fill status output from the level of the contents of the elastic store,

generating a first coefficient representative of the rate of byte justification in relation to the data byte rate,

combining the first coefficient with the store fill status output to provide an input to a local clock control circuit, and

controlling the frequency of the local clock thereby,

combining the output of the local clock with the bit justification information to produce a second control clock signal,

transferring the contents of the elastic store to a byte/bit converter under the control of the second control clock signal, and

controlling the output of the byte/bit converter to output the data at the frequency of the local clock.

In order that the invention may be readily understood an embodiment thereof will now be described in relation to the drawings, in which:

Figure 1 shows a clock filtering arrangement required for SDH equipment, in the form of a bandpass filter filtering an incoming reference clock frequency so that noise and sidebands outside the filter's passband are substantially attenuated and a cleaner clock signal is provided by the filtering

arrangement.

Figure 2 shows a block diagram illustrating implementation of the invention.

Figure 3 is a simplified timing diagram illustrating various functions of the invention.

Figure 4 shows a phase locked loop arrangement embodying the invention.

Figure 5 shows a transmission system in which the invention may be used.

Figure 6 illustrates bit justification.

Figure 7 illustrates byte justification.

To place the invention in context a brief discussion of a typical transmission system will be given by way of example.

Figure 5 shows a telecommunications system in which the invention may be applied. In Figure 5 a plurality of tributary data streams with a bit rate of fo are shown, are multiplexed and enter into the transmission system of T1. The data with frequency fo must be re-timed and formed into bytes at the transmission rate from T1 , ie. f1. This may require some "bit stuffing" at T1 for compatability. This will be discussed further in relation to the data multiframe and higher level data structures.

The data may pass through a series of data terminals (T2 ... Tn) each of which may have variations in its operating frequency. At each terminal these frequency variations are corrected by "byte stuffing" as discussed below.

When the original message sent at fo reaches the terminal Tn to which the station to which the message is addressed is connected, it is necessary to eliminate the bit and byte-stuffing to reconstruct the message at fo which is extracted by demultiplexing.

A typical multiframe structure for such a system is shown in Figure 6 and a higher order data structure built up from the contents of such multiframes is shown in Figure 7.

An example of how bit justification is achieved under CCITT G.709 is discussed with reference to Figure 6.

This figure shows a block of 140 bytes which include three frames each with a byte including bits C1 and C2. The last frame also includes bits S1 and S2 and these bits may be used to carry data or justification bits. The three bits C1 are used on a majority decision basis, to indicate whether S1 is data or justification, and the C2 bits do likewise for S2. Majority decision is used to reduce effects of one C1 or C2 pulse being corrupted. Thus at the receiving end bits C1 end C2 are used to indicate whether S1 and S2 are data or justification bits.

In Figure 6, 1 represents a normal information bit, 0 is a reserved bit, R is a fixed stuff bit, C is a justification control bit, and S is a justification opportunity bit.

Byte justification is discussed with reference to Figure 6, which shows an array of 4 frames each consisting of 270 x 9 bytes.

Within the first 9 columns of each frame row 4 is made up of a selection of bytes labelled H1, H2, H3, Y, and 1. An SDH system is designed to carry various types of data structures end the information carried in the byte justification location bytes H1, H2, H3 is adjusted according to the type of data being transmitted. The bytes H1 and H2 carry information identifying the justification bytes, or as in the embodiment shown, they indicate the end of the justification bytes. The H3 bytes are available for negative justification opportunities (Figure 7A), and these are followed by a similar number of bytes available for positive justification opportunities (Figure 7B).

Where there is a mis-match between the byte transmission rates of different segments of a transmission path, the justification bytes are used to correct the mis-match. To permit two-way adjustment, each group of four frames contains a number of justification opportunities which may be increased or reduced as required. This is illustrated by negative and positive justification as shown in Figures 5A and 5B.

In the SONET system a data channel may be a 2 Mbit/sec data stream. SONET which has a transmission rate of 155 Mbit/sec can carry 63 such channels together with "housekeeping" information. At the receiving end the data may be de-multiplexed to give an output containing the information from the 2 Mbit/sec input. However the form of this output is intermittent bursts of 155 Mbit/sec, eg. 8 bit bytes separated by varying time gaps. The variation in the time gaps is caused by byte justification, ie. the insertion or removal of dummy bytes to match the input data to the SONET transmission rate. In addition, byte lengths may vary (bit justification). Justification bits may occur in SONET every 4 bytes while up to 3 justification bytes may occur every 4 frames of 2430 bytes/frame.

The output clocking must be able to compensate for both types of justification but clearly there is much more time available to deal with the large corrections (8 bits/byte) required for byte justification, compared with the time available to correct for bit justification. The object of adjusting the output clock is to produce an output data rate in which both transitions can be achieved smoothly.

The smoother the changes in the output clock rate, the easier it is for the receiving equipment to track the changes.

As discussed above the basic SONET system provides two sources of clock adjustment, bit justification and byte justification. There are proposals for system which may have a plurality, eg. 5, different sources of clock adjustment and the invention can be applied also to such systems by

providing a suitable number of variations in the output clock algorithm.

Referring to Figure 1, a raw SDH clock signal, which may contain framing gaps and other distortions, has added to it byte justification information in a summing device 1. This modified clock signal is then used to load data into a byte elastic store 2 as well as being applied to a bandpass filtering device 3. The clock at the output of bandpass filtering device 3 has been rendered significantly cleaner by the filtering device and is utilised as a read clock to unload data from elastic store 2 from where it is forwarded to a parallel to serial converter 4 for conversion from bytes of data to a serial bit stream of data. At this point bit justification information is applied to both clock and data in summing device 5 and converter 4 respectively. The resultant clock signal from summing device 5 is used to load data from converter 4 into a second elastic store 6. The clock from summing device 5 is also applied to a second bandpass filtering device 7 so that a filtered clock is available at output 8. This clock is also used to output data from the second elastic store 6 and present it at data output 9.

It should be noted that in practical application the bandwidth of the second bandpass filtering device 7 is probably ten times that of the bandwidth of the first bandpass filtering device 3.

If the bandpass filtering devices shown in Figure 1 were replaced by phase locked oscillators it would be seen that the bandpass characteristic is generated by the lowpass characteristic of the phase locked loop components converted with the oscillator frequency by a phase discrimination device associated with the phase locked oscillators, to form a bandpass filter centred on the oscillator frequency. This results in considerable simplification of the bandpass filter circuit especially when narrow bandwidths are required.

In the clock filtering arrangement described in relation to Figure 1, all filtering is applied to the SDH clock signal and SDH data is smoothed by these clock signals in the associated FIFO type elastic stores 2, 4 and 6.

With respect to filter design generally, there are a number of methods known in the art by which a specified filtering function may be obtained. These methods include, for analogue designs, lattice or ladder configurations; and for digital designs, transversal or recursive in single or cascaded configurations, or combinations of both analogue and digital configurations. The present invention may use a combination of digital configurations as the preferred option.

With reference to Figure 2, data at the system transmission rate eg. 155 Mbits/sec is demultiplexed in demultiplexer 101 into a plurality of channels, eg. 63 channels. The data for each channel is then contained in irregularly spaced bursts of data at 155 Mbit/sec. The invention will be described in relation to one such channel.

Byte justification identification means 102 use the byte justification identification information contained in the data stream to identify the justification bytes. The output of this circuit is combined with the output of the byte clock detector 102 in byte clock gating means 104 to produce a write clock which is stripped of justification byte pulses. This write clock is used to control the input to buffer store means 105. This ensures that only bytes containing genuine information are admitted to the store 105.

Store 105 includes means to measure the contents of the store and to provide a signal on line 107 indicating the level of the contents. In a preferred embodiment this may have an accuracy of 1/4 bit.

A particular level of contents of store 105 is selected as the datum level, eg. half full and the contents signal is used to control the oscillator controller 108 to cause the frequency of the oscillator controller 108 to cause the frequency of the oscillator 109 to increase or decrease depending on the contents of the store 107.

Bit justification identification means 110 is fed with the input data bytes and identifies when a justification bit is received. This information is combined with the output of oscillator 109 in byte length control 111 to provide a read clock on line 112 for store 105 with a duration which can be varied between 7 and 9 pulses of output oscillator 109. Line 112 may have 2 wires to indicate byte length.

On receipt of a read clock pulse a byte of the appropriate length is read into parallel-to-serial converter 113 and is read out of the converter 113 under the control of oscillator 109 via line 114. Thus the smoothed data appears on line 115 and the output clock on line 116.

Oscillator control 108 can operate in two or more different modes and may be implemented by a coefficient generator. In the case where there are only two sources of clock adjustment, ie. byte and bit justification, the output of, eg., the justification byte identification means 102 is applied to control 108 via line 117 to identify when a justification byte adjustment is required, and cause control 108 to make the required adjustment to oscillator 109.

In the event of a justification bit being received this will be detected by the store contents measuring means and indicated on line 107. The oscillator control 108 will recognise this as a justification bit because of the absence of a justification byte signal on line 117, and control 108 will cause an adjustment to oscillator 109 appropriate for a jus-

tification bit.

Thus the circuit is able to make different adjustments to the output clock from oscillator 109 depending on the cause of the need for adjustment. The system can be adapted to deal with a plurality of sources of clock adjustment which can be identified in the same way as bit and byte justification. The timing diagram of Figure 3 is illustrative of the operation of the arrangement shown in Figure 2. The byte clock detector (BCD) 103 detects the start of each byte and generates a pulse for each byte as shown in line (i). Justification bytes are identified in justification byte identifier (JBI) 102 (line ii) and gated with the output of BCD 103 to produce the write clock (line 4) for buffer 105, and this controls the data to be written into buffer 105, causing justification bytes to be excluded. The output from JBI 102 is applied via line 117 to oscillator controller 108 and notifies it that the consequent drop in contents of buffer 105 as notified to controller 108 is due to a justification byte and thus the controller 108 adjusts the oscillator 109 frequency accordingly. The bytes are thus fed out of buffer 105 at a slower rate and this is illustrated in line (iv) by showing eg. 6 write pulses spread over the time which the data and justification bytes occupied in line (i). In reality this adjustment may be spread over several frames in an SDH system so only small incremental changes in the output of oscillator 109 are required. Line (v) illustrates that the incoming data bytes may have 8 +/- 1 bits.

As shown in line (vi), if an incoming byte has 8 bits then there should be no change in the contents of buffer 105 to cause oscillator 109 to be adjusted. However, if an input byte has 9 bits this is detected at 107 and the controller 108 would interpret this as a justification bit in the absence of a signal on line 117 so that oscillator 109 is adjusted at the appropriate rate for bit justification as determined by the operating rules for the transmission system.

Referring to Figure 4, byte justification information is combined with raw SDH clock signal in a summing device 1 and the result is used as the write clock for a byte elastic store 2. Thus justification bytes are blocked from entering the store. The byte justification information is also made available to a byte filter coefficient block 3 and a signal therefrom is combined with elastic store fill status information in summing device 4. The elastic store fill status information is a measure of the difference in the rates at which data is read into and out of the store. Summing device 1, byte elastic store 2, first filter coefficient generator 3 and summing device 4 form a transversal filter whose output is coupled to a phase locked loop filter coefficient device 5. The output of filter coefficient device 5 provides control information to a controlled oscillator (cf. a VCO) 6 which provides a read clock for a byte/bit converter 7 and the byte elastic store 2, thereby unloading the data for presentation at SDH data output 9. The read clock for the elastic store may be produced by a signal from the byte/bit converter indicating that the converter is ready to receive the next byte. Bit justification information is fed to converter 7 and reflects in the byte store 2 fill status which is applied to the phase locked loop elements comprising summing device 4, second coefficient generator 5 and oscillator 6. Bit justification information can vary size of bytes, eg. 8 +/- 1, and by speeding/slowing read clock for byte elastic store 2 to change the rate at which data is read from 2 into Byte/bit converter 7.

The filter formed by the first summing device 1, byte elastic store 2, first coefficient generator 3 and second summing device 4 has a bandpass characteristic like that used for bandpass filtering device 3 of Figure 1. Similarly, the filter formed by the byte elastic store 2, second summing device 4, second coefficient generator 5, VCO 6 and converter 7 have filter characteristics like those of the second bandpass filtering device 7 of Figure 1.

It will be understood that the order of summing the independent justification sources may be of any order. For example, the justification shown in converter 7 could be injected prior to summing device 1.

The techniques described in relation to the arrangement of Figure 4 can be adapted to other arrangements which provide filtering for any number of independent sources of information such as, for example, monitoring sources providing a plurality of independent factors in any process.

Regarding the filtering responses, any filter response which uses the separate filtering component arrangement described in relation to Figure 1 is also possible with the combination filter arrangement described in relation to Figure 4.

While the present invention has been described with regard to many particulars it is to be understood that equivalents may be readily substituted without departing from the scope of the invention.

Claims

1. A method of extracting a smoothed output clock from an input data stream including specific data and two or more sources of clock adjusting signals the method including identifying the source of each of the clock adjusting signals,

applying the input data stream to retiming means,

generating an output clock signal to control the read rate, being the rate at which the

specific data is fed out of the retiming means,

comparing the average of the write rate, being the rate at which the specific data is fed into the retiming means with the average of the read rate,

adjusting the output clock signal so that the average of the read rate approximates the average of the write rate,

wherein the output clock signal is adjusted at a rate of adjustment determined by the identity of the source of the clock adjusting signal.

2. A method as claimed in claim 1 wherein when a first source of clock adjustment signals is identified the corresponding data is prevented from entering the retiming means.

3. A method as claimed in claim 1 wherein when a first source of clock adjustment signals is identified the corresponding data is prevented from being fed out of the retiming means.

4. A method as claimed in any one of claims 1 to 3 wherein the retiming means comprises a buffer store feeding into a parallel-to-serial converter.

5. A method as claimed in claim 4 wherein the comparison of the average read rate with the average write rate is carried out by measuring the contents of buffer store.

6. A method as claimed in claim 4 or claim 5 wherein the input data stream includes justification bytes, justification bits, justification byte identification information, and justification bit identification information, wherein data is fed from the buffer store to the parallel-to-serial converter means in variable length bytes, and wherein the justification bit identification information is used to control the length of said variable length bytes.

7. A method of obtaining a smoothed output data flow from an input data stream including two or more sources of clock adjusting signals the method including extracting a smoothed output clock signal by the method of any one of claims 4 to 6 and using the smoothed output clock as a read clock to read the data out of the parallel-to-serial converter.

8. A method of extracting output data from a stream of pulses containing data bytes, justification bytes and justification bits, justification bit identification information and justification byte identification information, the method comprising:

buffer store means as they are received, blocking the justification bytes from entering the buffer store means,

measuring the contents of the buffer store means to produce a store fill status signal,

using the store fill status signal to control the frequency of an output clock signal,

feeding the data out of the buffer store means at a rate controlled by the output clock signal,

wherein the justification byte information is used to block the justification bytes from the buffer store means,

wherein the buffer store means operates as a FIFO store,

wherein the data from the buffer store means is fed to a parallel-to-serial converter in bytes, and wherein the number of bits per byte is controlled by the bit justification information,

wherein the frequency of the output clock signal is controlled by the store fill status signal so as to tend to maintain the contents of the buffer store means at a chosen level.

9. An output clock filter arrangement for obtaining a smoothed output clock from a data stream including specific data and two or more sources of clock adjusting signals,

the arrangement including identification means to identify corresponding sources of clock adjusting signals,

retiming means into which the data stream is fed,

output clock generating means including a controllable oscillator controlled by oscillator control means,

comparator means to compare the average of the write rate, being the rate at which the specific data is fed into the retiming means with the average of the read rate, being the rate at which the specific data is read out of the retiming means,

the comparator means controlling the oscillator control means so that the average read rate approximates the average write rate,

and wherein the oscillator controller adjusts the frequency of the oscillator at different rates of adjustment in accordance with the identity of the source of clock adjusting signals.

10. An arrangement as claimed in claim 9 including first gating means responsive to a first of the sources of clock adjusting signals being identified to prevent data associated with said first Of the sources from entering the retiming means.

11. An arrangement as claimed in claim 9 or claim 10 wherein the retiming means comprises a buffer store feeding into a parallel-to-serial converter.

12. An arrangement as claimed in claim 11 wherein the comparison means comprises means to measure the level of the contents of the buffer store.

13. An arrangement as claimed in any one of claims 11 to 12 wherein the data stream includes justification bytes, justification bits, justification byte identification information and justification bit identification information, the arrangement including byte control means to control the number of bits per byte fed from the buffer store to the parallel-to-serial converter in response to the justification bit identification information.

with reference to Figures 2 to 7 of the accompanying drawings.

14. Apparatus for extracting smoothed output data from a data stream including specific data and two or more sources of clock adjusting signals,

the apparatus including an output clock filter arrangement as claimed in any one of claims 10 to 13 wherein the output of the oscillator is used as the read clock to control the output of the parallel-to-serial converter.

15. A method of providing a controlled response from each Of a plurality of clock sources to a single controlled oscillator means using independently sensed information signals from each clock source, each clock source contributing to a total data process forming a data stream whose rate requires filtering by the controlled oscillator means, said method comprising the steps of:

1) Monitoring each said clock source for transient conditions.

2) Generating a response characteristic for each monitored clock source.

3) Combining the results of the characteristics so generated to obtain a total modifying function.

4) Obtaining a total phase difference signal between the data stream to be filtered and the controlled oscillator means' output.

5) Combining the total modifying function with the total phase difference to produce a modified phase function.

6) Processing the modified phase function to produce a control signal for application to said controlled oscillator means.

16. A method for adjusting the local clock data rate to accommodate the data rate of an incoming data stream which includes byte justification information and bit justification information, the method comprising:

combining the byte justification information to the incoming data byte clock information to produce a first control clock signal,

storing the incoming data in an elastic store under the control of the first control clock signal,

deriving a store fill status output from the level of the contents of the elastic store,

generating a first coefficient representative fo the rate of byte justification in relation to the data byte rate,

combining the first coefficient with the store fill status output to provide an input to a local clock control circuit, and

controlling the frequency of the local clock thereby,

combining the output of the local clock with the bit justification information to produce a second control clock signal,

transferring the contents of the elastic store to a byte/bit converter under the control of the second control clock signal, and

controlling the output of the byte/bit converter to output the data at the frequency of the local clock.

17. An arrangement for adjusting the local data rate to accommodate the data rate of an incoming data stream which includes byte justification information and bit justification information, the arrangement comprising:

first adder means for adding the byte justification information to the incoming data byte clock information,

the output of the first adder means being applied to byte elastic store means as the byte input clock,

the data from the incoming data stream being fed into the elastic store means under the control of the byte input clock,

the byte elastic store including a store fill status output indicating the level of the contents of the elastic store,

the byte justification information being applied to a first coefficient generator which produces an output corresponding to the number of insertions of justification bytes in relation to the data byte rate,

combining means to combine the output of the first coefficient generator and the store full status output,

the output of the combining means being applied to a second coefficient generator which

controls the frequency of a local clock oscillator to bring the frequency of the local clock oscillator closer to synchronism with the bit clock rate of the incoming data,

the output of the local clock oscillator is combined with the bit justification and controls the reading of data from the elastic store into a byte/bit converter,

the data being read from the byte/bit converter under the control of the output of the local clock oscillator.

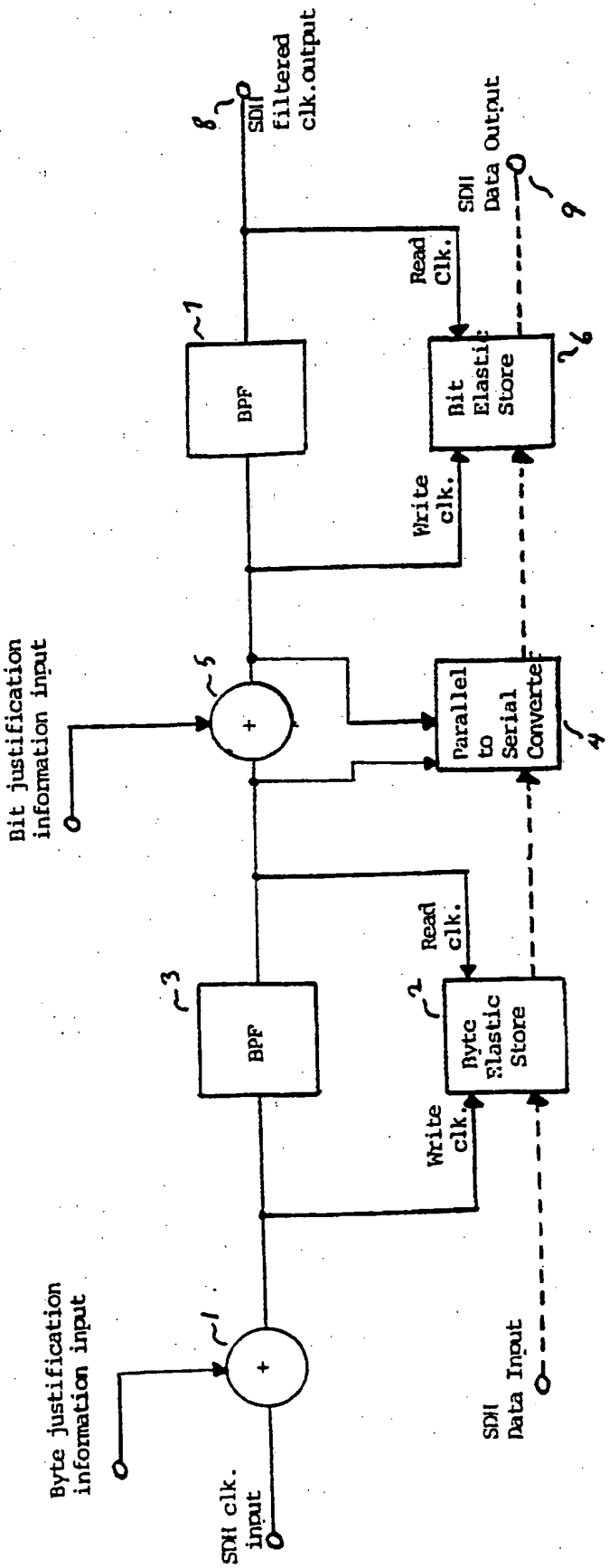
SDH clk. input
Byte justification information input
Bit justification information input
SDH Data Input
SDH Data Output
SDH filtered clk.output
Write clk.
Read clk.
Byte Elastic Store
Bit Elastic Store
Parallel to Serial Converter
BPF
BPF
+
+
1
2
3
4
5
6
7
8
9

Fig 1.

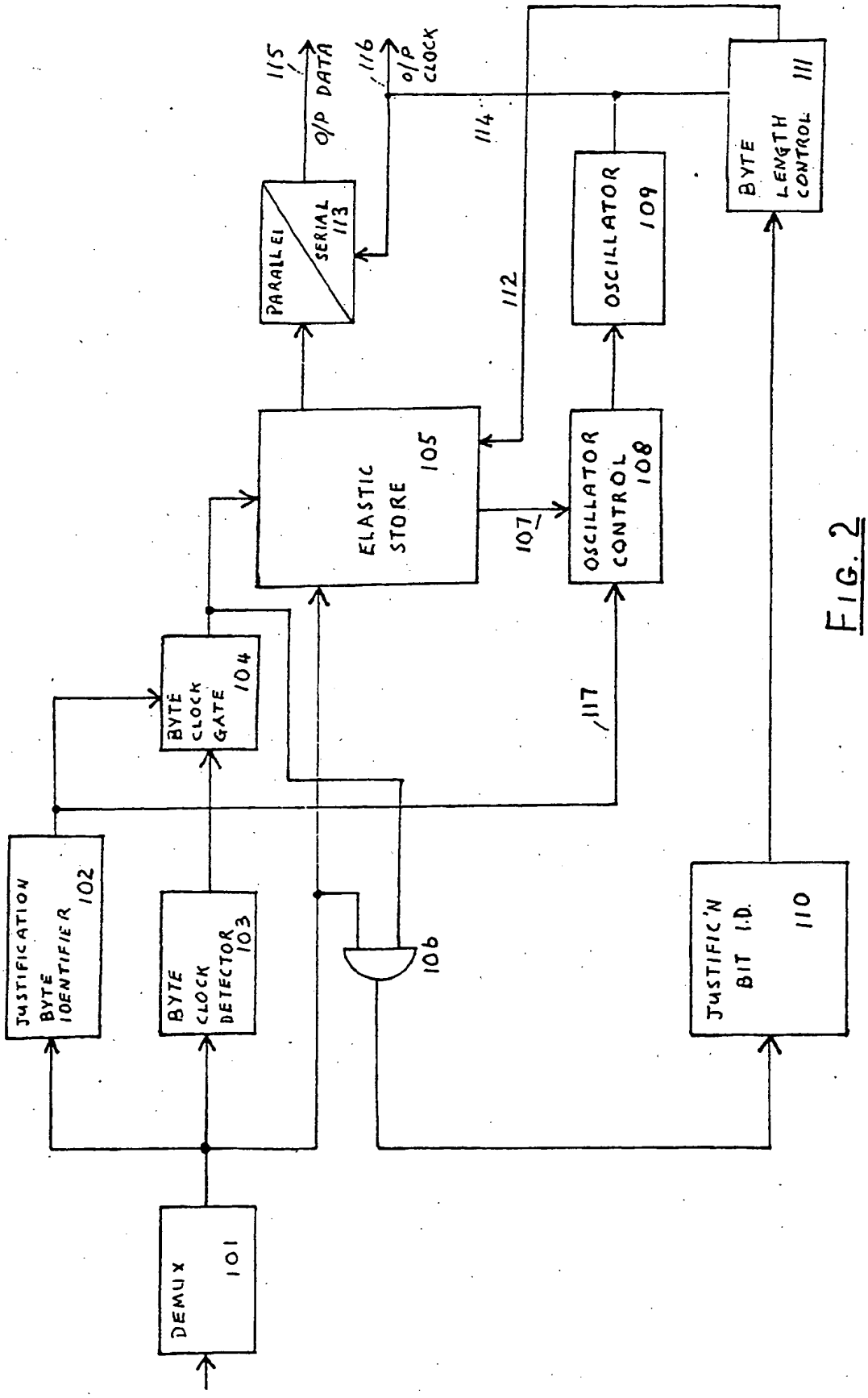
DEMUX
101
JUSTIFICATION BYTE IDENTIFIER
102
BYTE CLOCK DETECTOR
103
BYTE CLOCK GATE
104
ELASTIC STORE
105
106
OSCILLATOR CONTROL
108
OSCILLATOR
109
JUSTIFIC'N BIT I.D.
110
BYTE LENGTH CONTROL
111
112
114
PARALLEL
SERIAL
113
115
O/P DATA
116
O/P CLOCK
117
107

FIG. 2

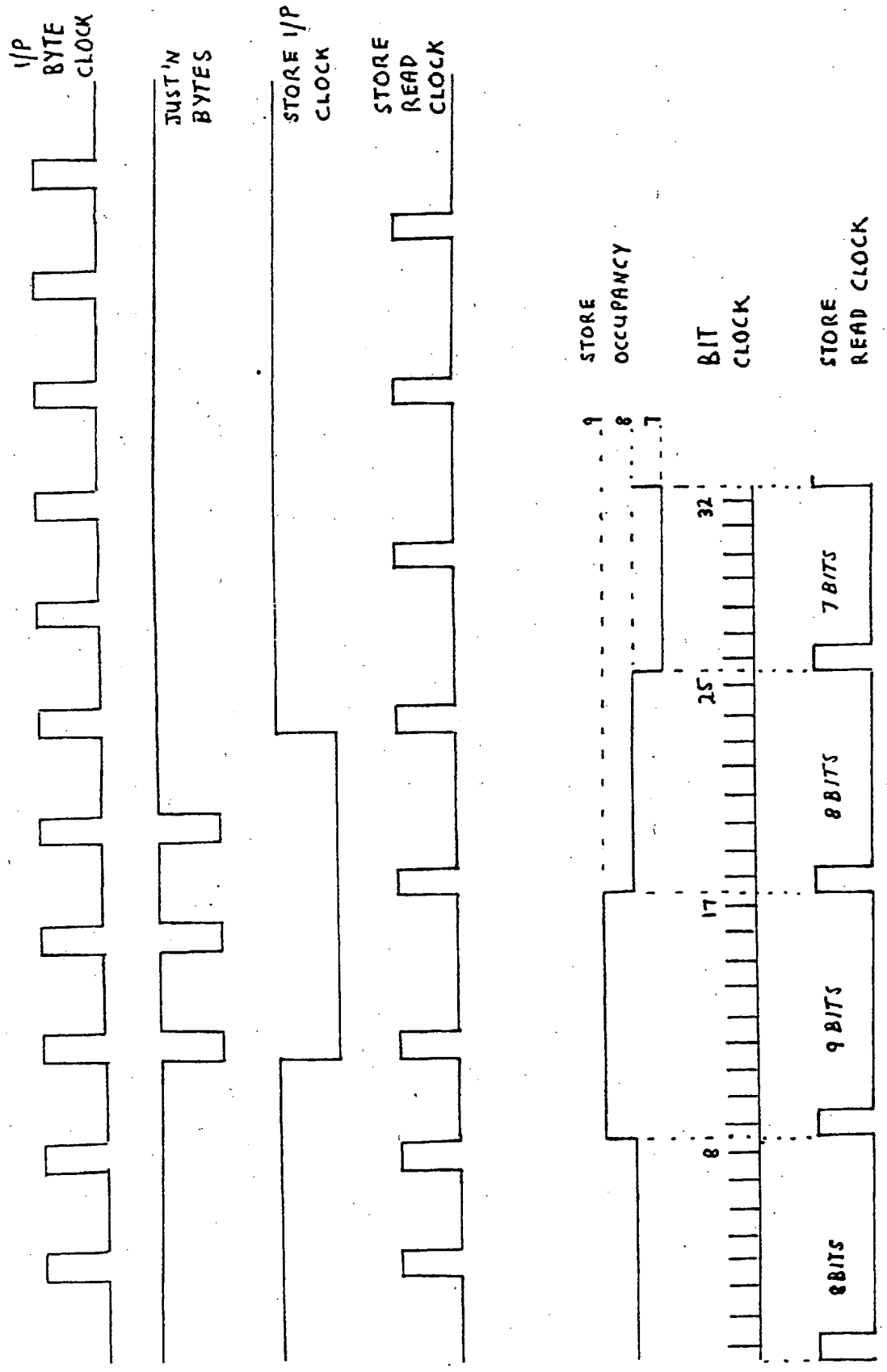
I/P BYTE CLOCK
JUST'N BYTES
STORE I/P CLOCK
STORE READ CLOCK
STORE OCCUPANCY
BIT CLOCK
STORE READ CLOCK
9
8
7
32
25
17
8
8 BITS
9 BITS
8 BITS
7 BITS

Fig. 3.

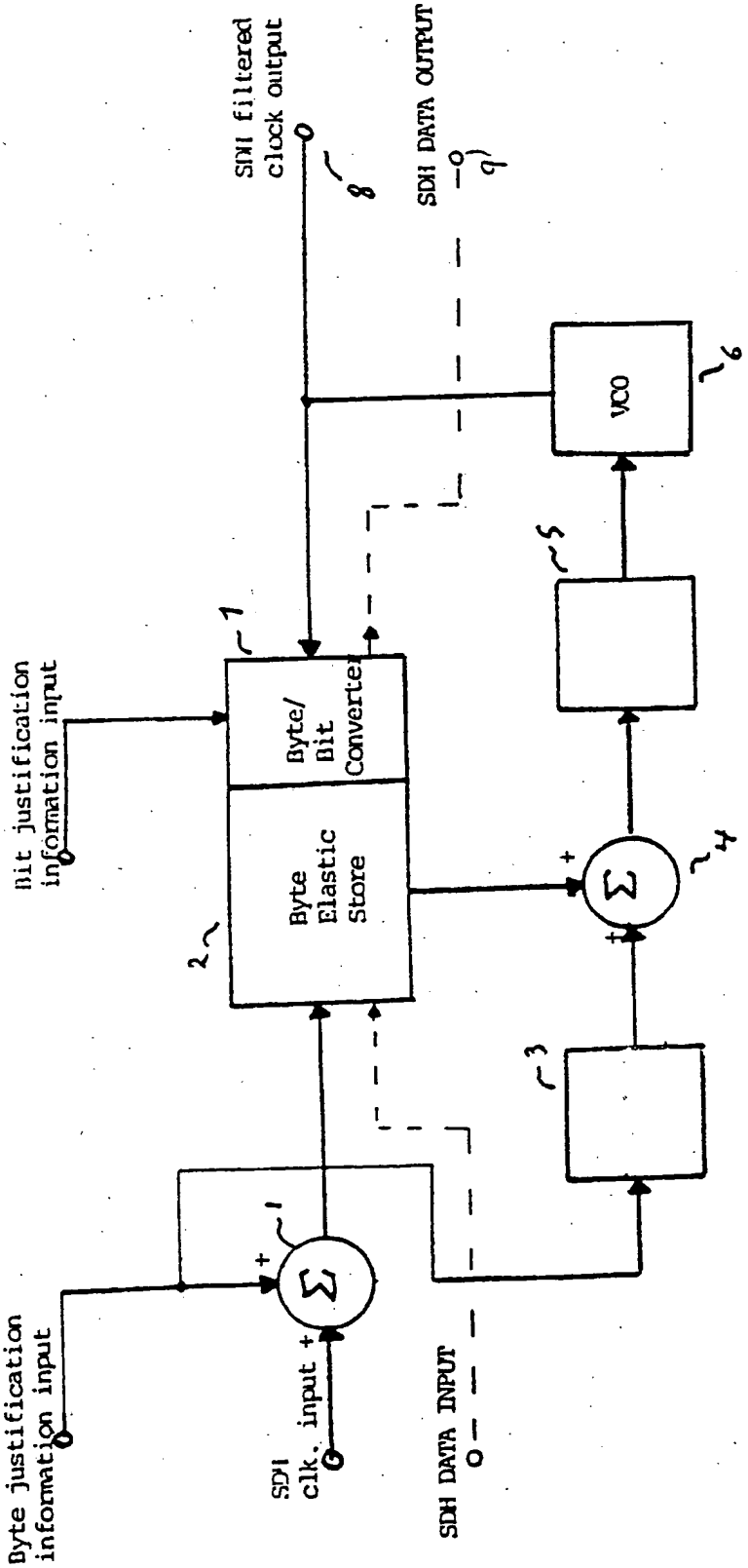
SDH filtered clock output
SDH DATA OUTPUT
VCO
Bit justification information input
Byte/ Bit Converter
Byte Elastic Store
Byte justification information input
SDH clk. input
SDH DATA INPUT

Fig. 4

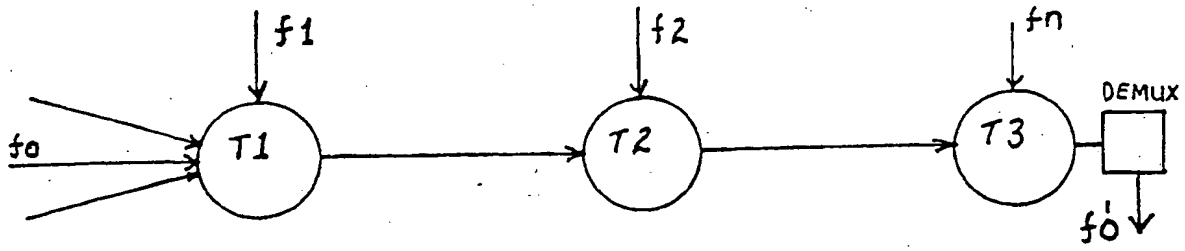

FIG. 5

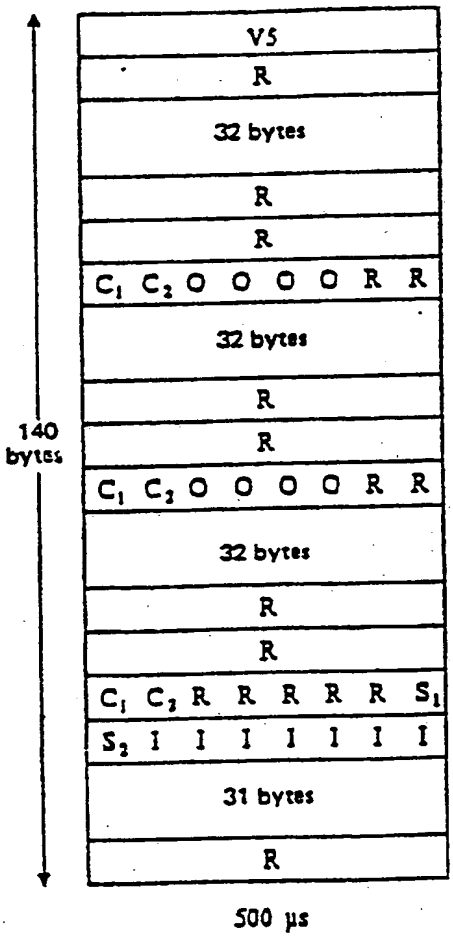

FIG. 6

I Information bit
O Overhead bit
C Justification control bit
S Justification opportunity bit
R Fixed stuff bit(s)

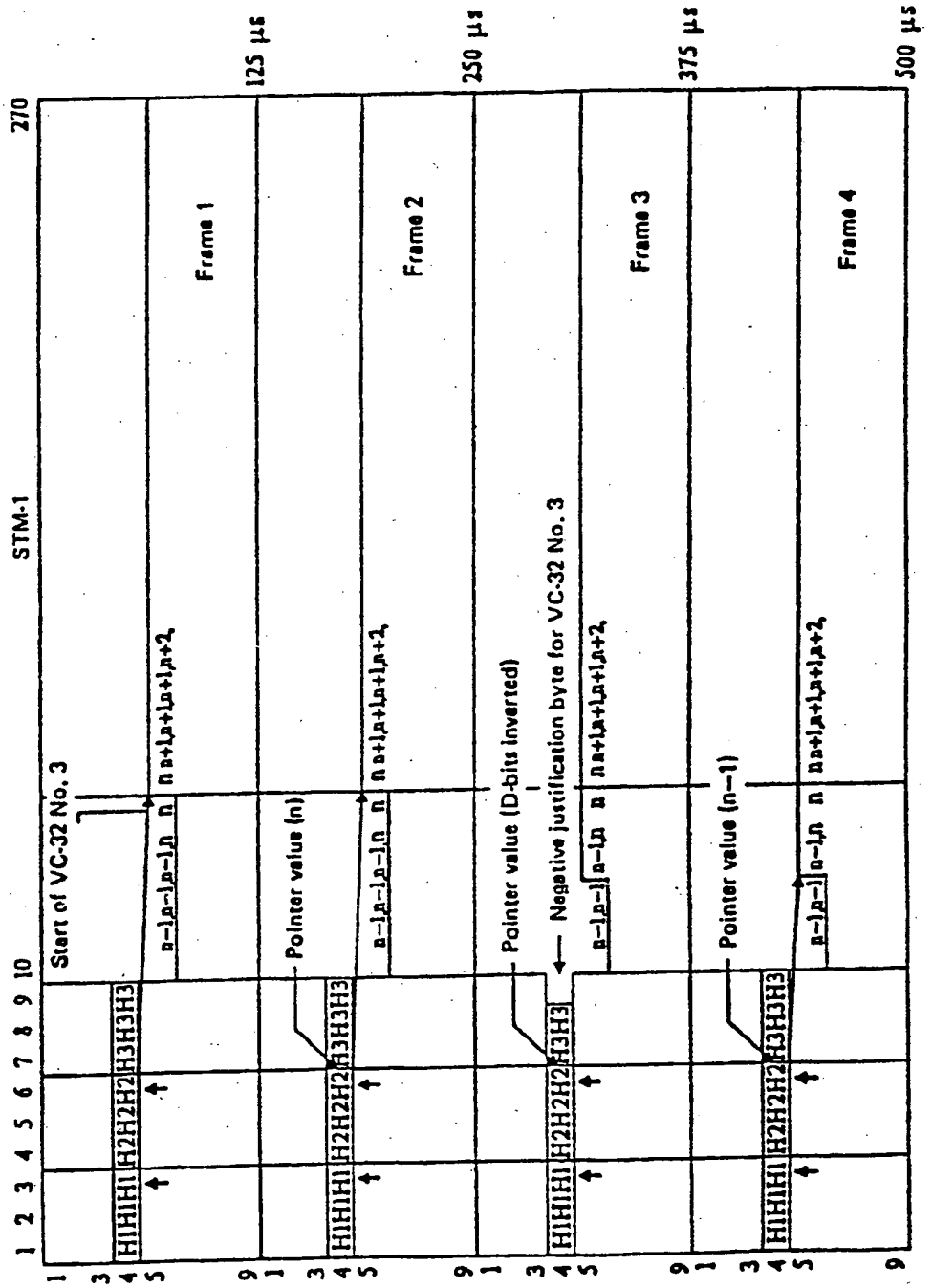
1 2 3 4 5 6 7 8 9 10
270
STM-1
125 µs
250 µs
375 µs
500 µs
Start of VC-32 No. 3
Frame 1
Frame 2
Frame 3
Frame 4
Pointer value (n)
Pointer value (D-bits inverted)
Negative justification byte for VC-32 No. 3
Pointer value (n−1)
H1H1H1 H2H2H2 H3H3H3
n−1 n−1 n n+1 n+1 n+1 n+2
↑: Indicates pointer operating on the VC-32 No. 3.

FIG. 7A

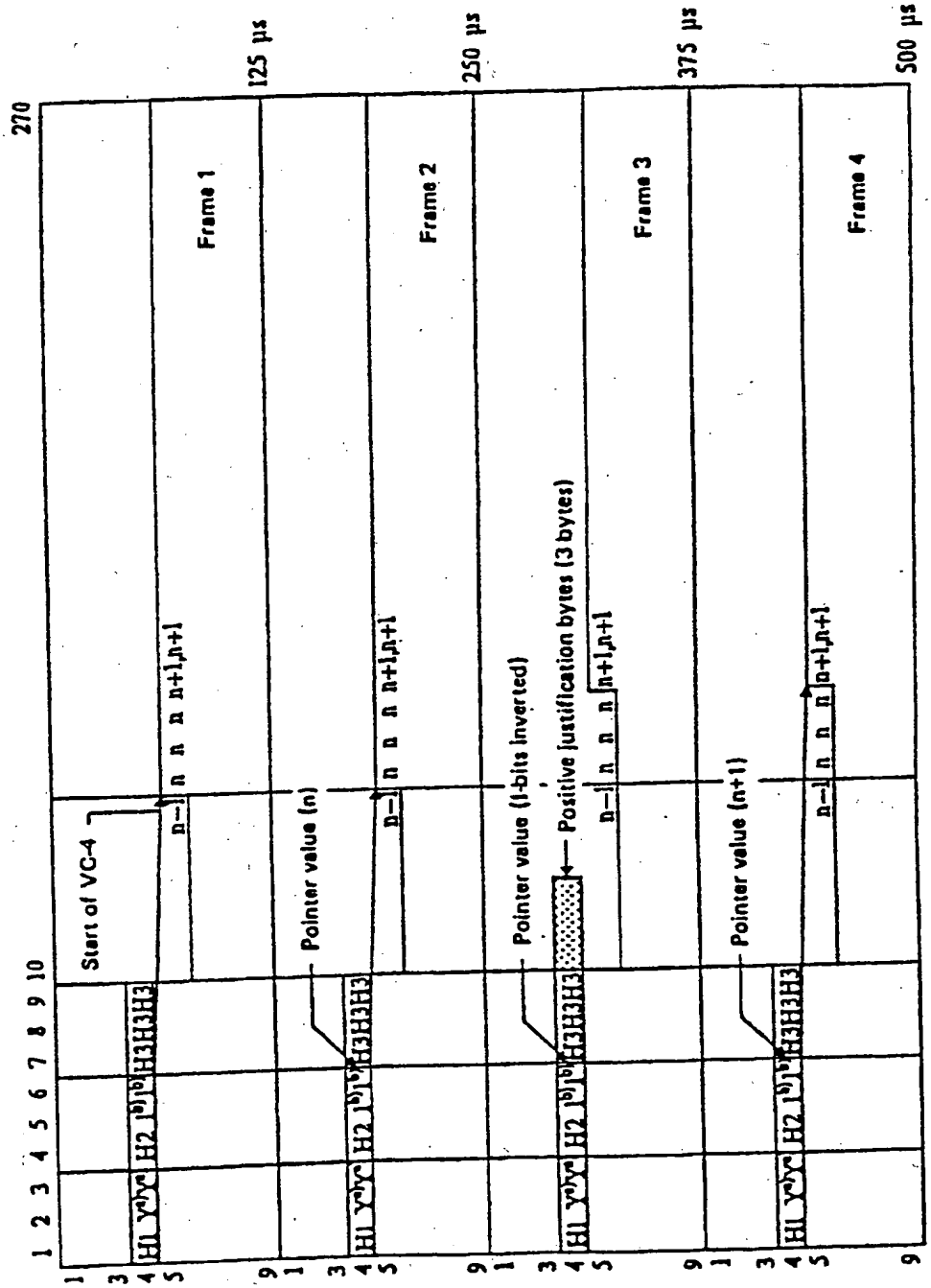

FIG. 7B

a) Y byte = 1001SS11 (S bits are unspecified).
b) All 1s byte.